

MT30046S

N-Channel Power MOSFET

30V,90A,4.6mΩ

Features

- $R_{DS(on)} = 4.6\text{m}\Omega$ at $V_{GS} = 10\text{V}$, $I_D = 30\text{A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

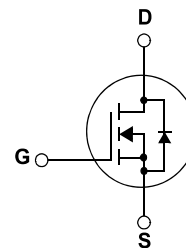
- DC-DC primary bridge
- DC-DC Synchronous rectification
- Hot swap



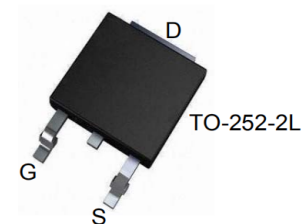
MT Semiconductor®

<http://www.mtsemi.com>

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Absolute Maximum Ratings T _A =25°C unless otherwise noted					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage		V _{DS}	30	V	
		V _{GS}	±20	V	
Continuous Drain Current ^G	T _C =25°C	I _D	90	A	
	T _C =100°C		40		
Pulsed Drain Current ^C		I _{DM}	150		
Avalanche Current ^C		I _{AR}	30	A	
Repetitive avalanche energy L=0.3mH ^C		E _{AR}	135	mJ	
Power Dissipation ^B	T _C =25°C	P _D	50	W	
	T _C =100°C		25		
Power Dissipation ^A	T _A =25°C	P _{DSM}	3	W	
	T _A =70°C		2.1		
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 175	°C	

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10\text{s}$	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
	Steady-State		41	50	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	Steady-State	$R_{\theta JC}$	2.1	3	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
MT30046S	MT30046S	TO-252	-	-	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.4	2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	150			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=30\text{A}$ $T_J=125^\circ\text{C}$ $V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		4.6 6.2 7.8	5.5 8.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$		49		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=12.5\text{V}$, $f=1\text{MHz}$		2050	2460	pF
C_{oss}	Output Capacitance			485		pF
C_{rss}	Reverse Transfer Capacitance			280		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		0.86	1.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $I_D=20\text{A}$		34	41	nC
$Q_g(4.5\text{V})$	Total Gate Charge			17	22	nC
Q_{gs}	Gate Source Charge			5		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $R_L=0.68\Omega$, $R_{GEN}=3\Omega$		7.5		ns
t_r	Turn-On Rise Time			11		ns
$t_{D(off)}$	Turn-Off DelayTime			27		ns
t_f	Turn-Off Fall Time			8		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		30	36	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		19		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300 \mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in ² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating. Rev1: March 2006

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

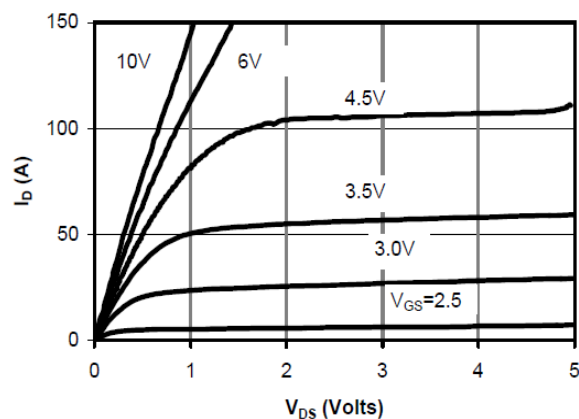


Fig 1: On-Region Characteristics

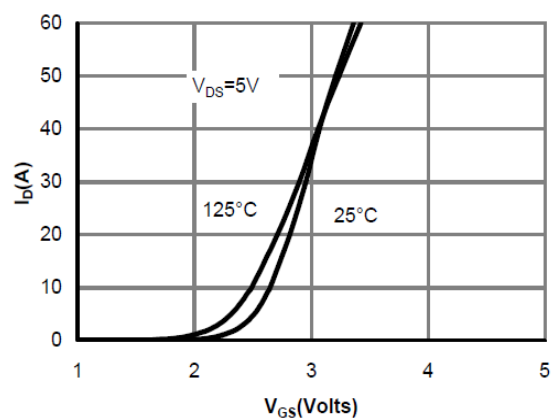


Figure 2: Transfer Characteristics

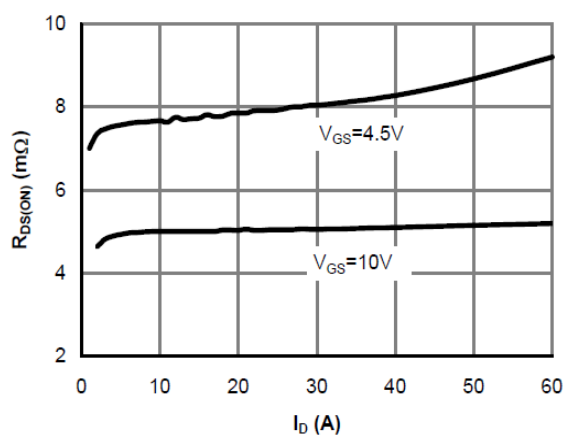


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

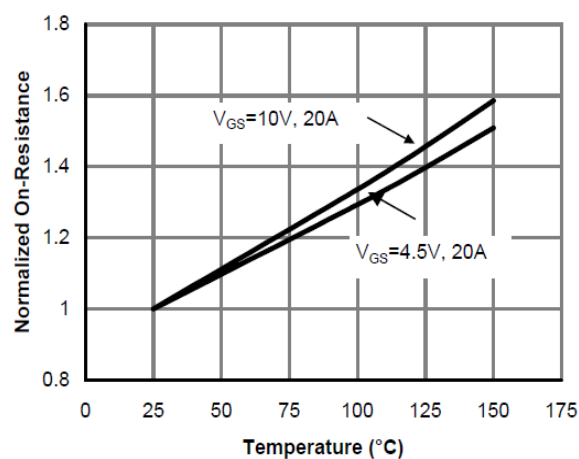


Figure 4: On-Resistance vs. Junction Temperature

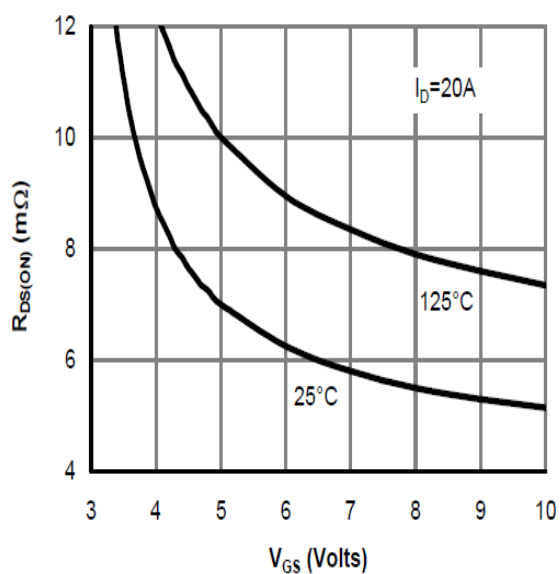


Figure 5: On-Resistance vs. Gate-Source Voltage

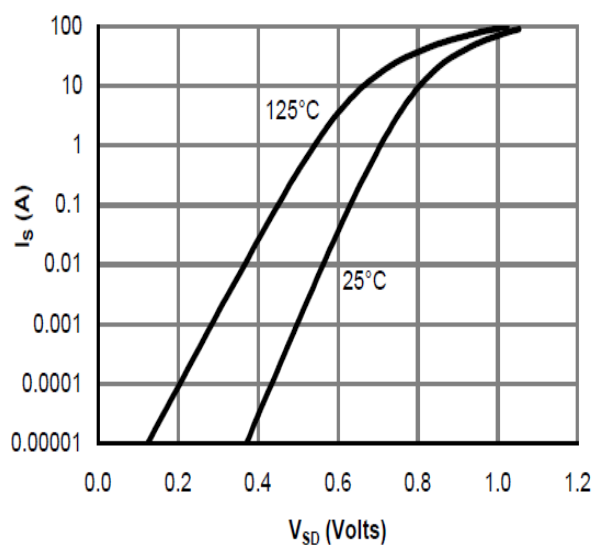
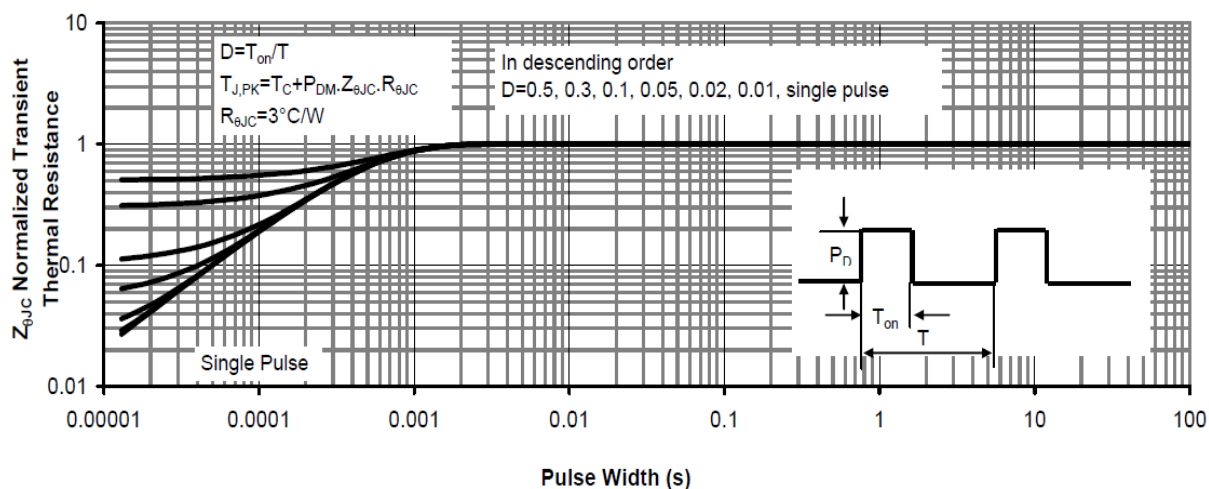
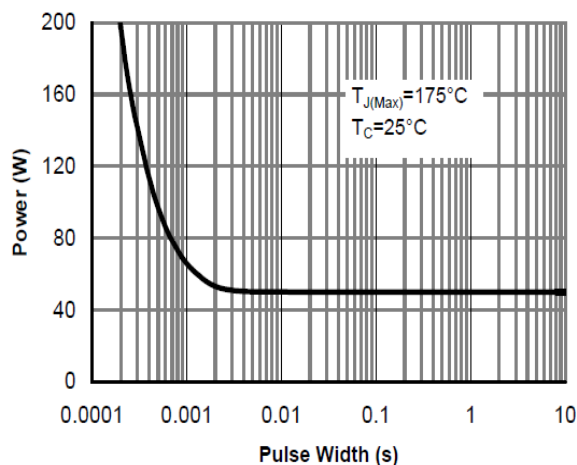
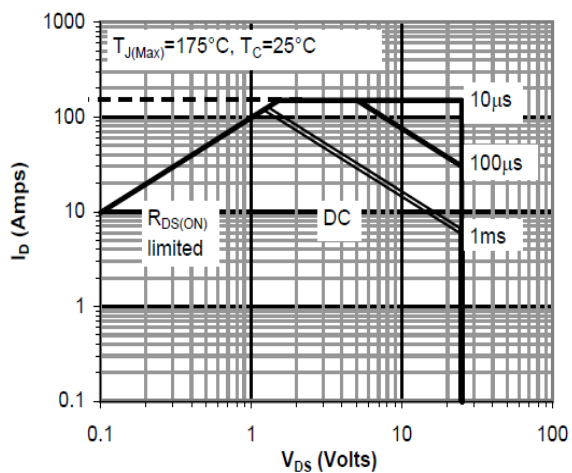
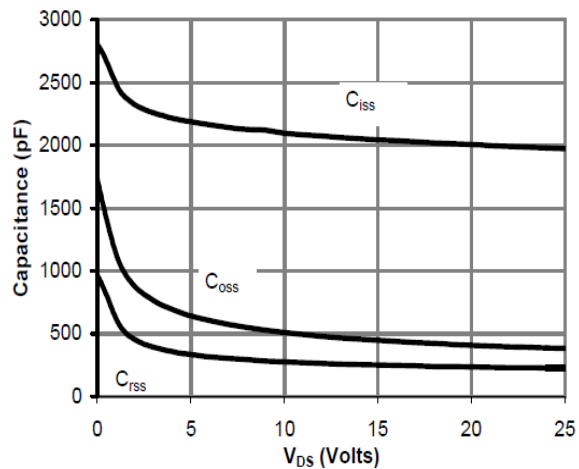
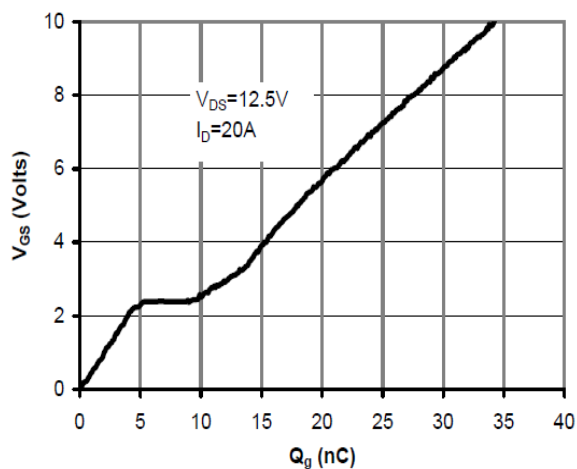


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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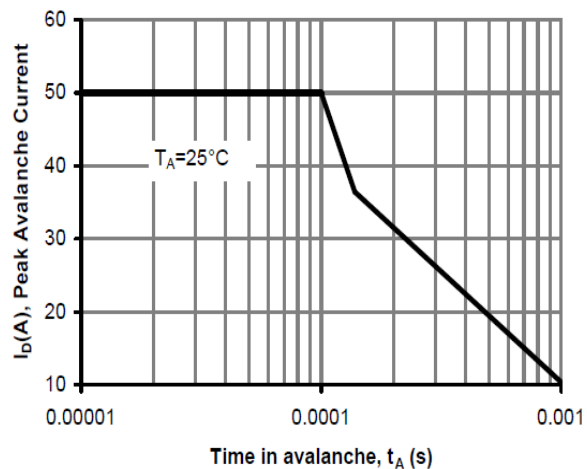


Figure 12: Single Pulse Avalanche capability

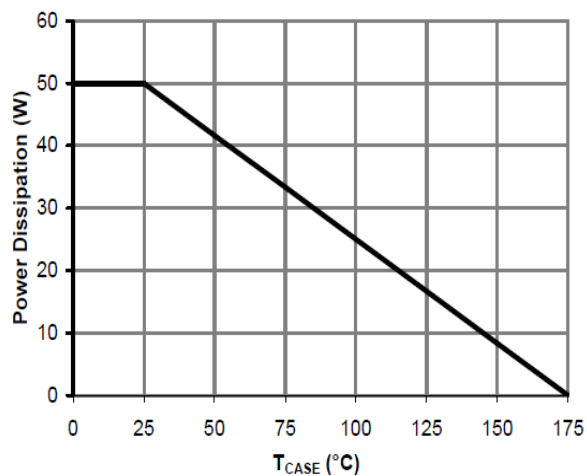


Figure 13: Power De-rating (Note B)

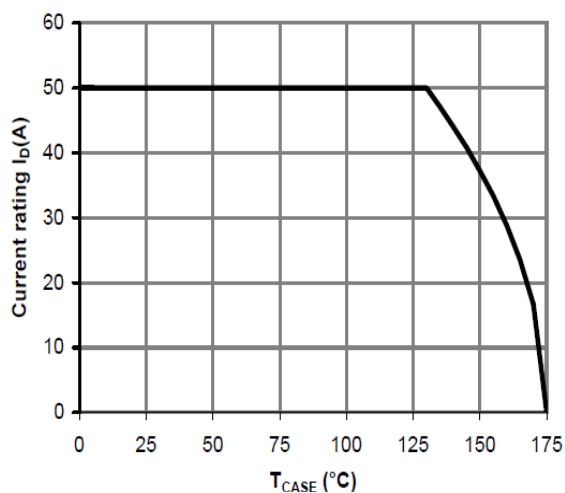


Figure 14: Current De-rating (Note B)

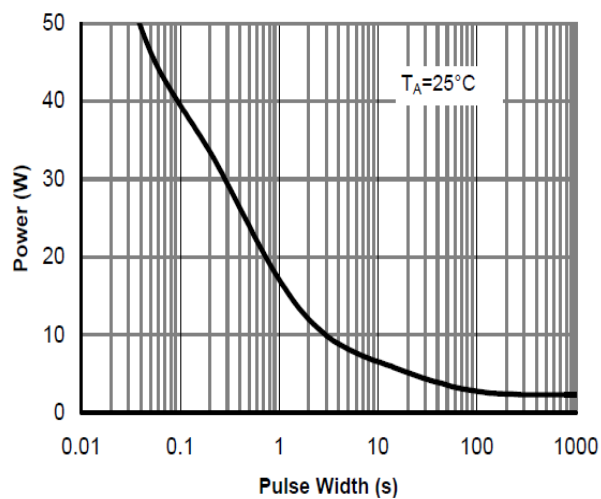


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

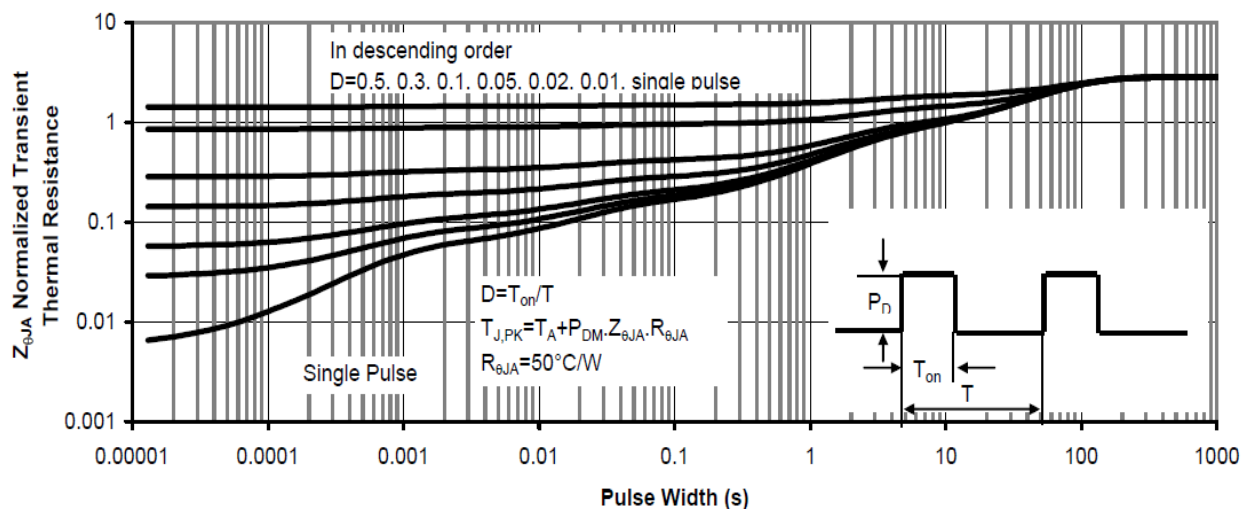
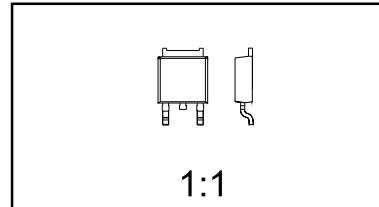
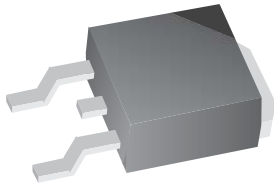


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Package Dimensions

TO-252-2L

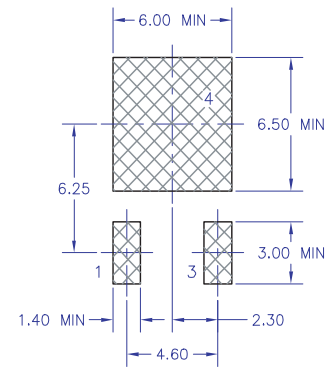
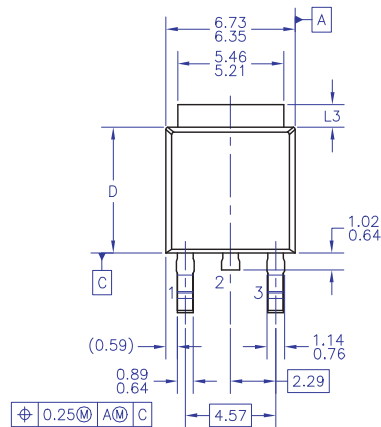


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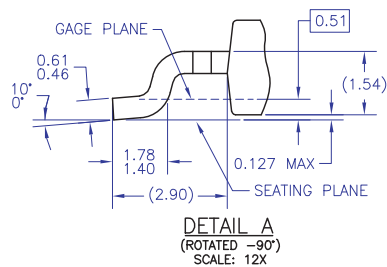
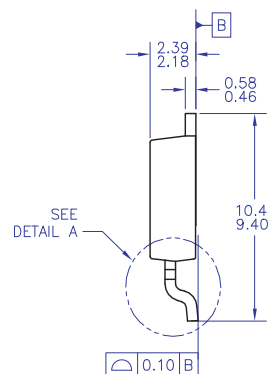
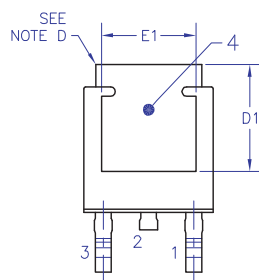
Scale 1:1 on letter size paper

Dimensions shown below are in:
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION

DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

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